P4-to-FPGA: Generating High Speed Network Devices

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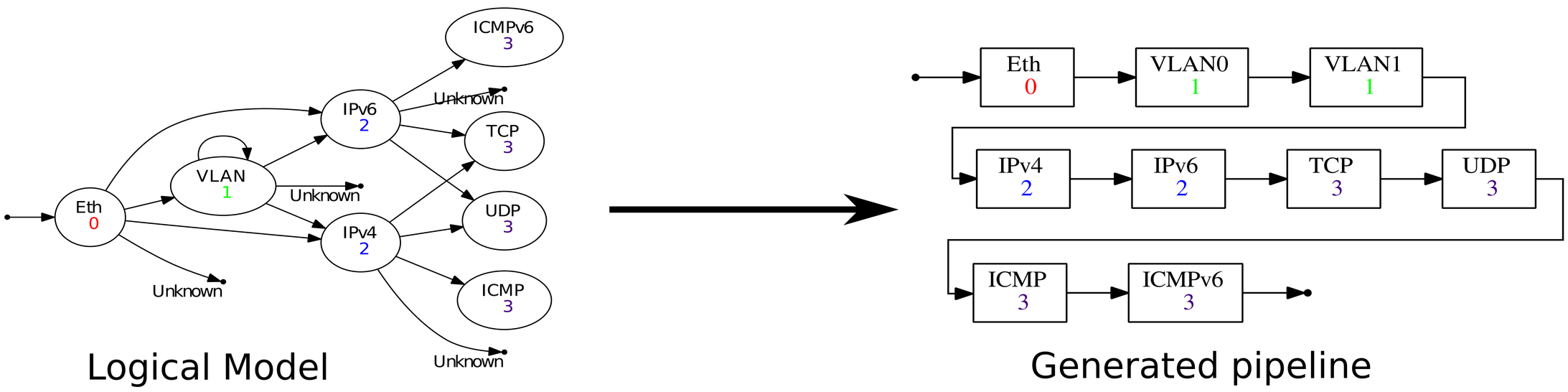
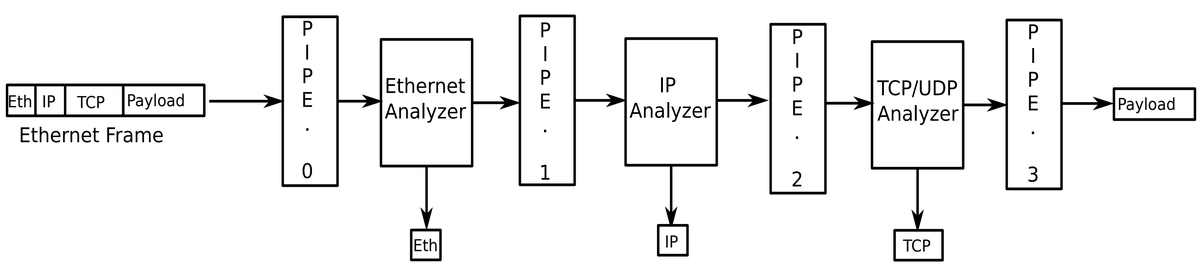
- Direct generation of parser and deparser blocks from P4 description
- Generated VHDL modules are capable to process 100 Gbps
- **Main idea**: mapping of the acyclic oriented graphs to a liner pipeline of processing elements (use DFS and find longest path from root to node)
- Both architectures (parser and deparser) are inspired by a hand-written code

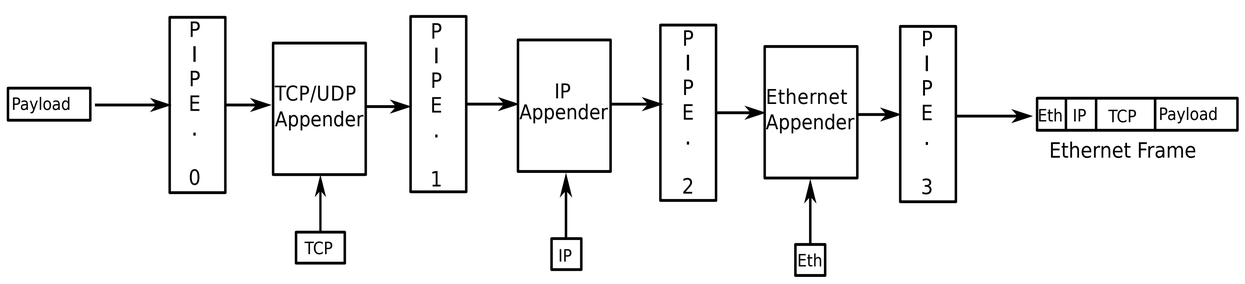
Example of the Parser Transformation



Architecture of Parser



Architecture of Deparser



Experiments

- **Simple L2**: Ethernet, IPv4/IPv6 (2×ext. headers), TCP/UDP, ICMP/ICMPv6
- **Full**: Ethernet, 2×VLAN, 2×MPLS, IPv4/IPv6 (2×ext. headers), TCP/UDP, ICMP/ICMPv6
- Xilinx Vivado 2015.1, Virtex-7 XCVH580T FPGA